Remarks

Claims 1-22 are pending, with claims 1, 9, 13, and 21 being in independent form. By the present amendment, claims 1, 9, 13, and 21 have been amended to correct an apparent typographical error.

In the Office Action, claims 1-22 stand rejected under 35 U.S.C. § 112, first paragraph.

Applicant describes a phase-locked loop that includes a phase detector, a loop filter, a voltage controlled oscillator and a frequency divider arranged such that the phase detector generates a phase detector output signal as a function of a phase difference between the reference clock signal and the feedback signal. The phase-locked loop further includes one or more circuit elements that maintain an operating point of the phase detector such that, for a predetermined range of both positive and negative phase differences between the reference clock signal and the feedback signal, the output signal is generated as a substantially linear function of the phase difference between the reference clock signal and the feedback signal. As defined by amended claim 1, the substantial linearity of the output signal is due at least in part to a shifting of the operating point so that a nonzero output signal corresponds to a nonzero phase difference between the first and second signals.

The operating point circuit may assume any of a number of alternative embodiments. For example, the operating point circuit may leak a predefined portion of the output signal so as to prevent the leaked output signal from influencing the output frequency of the phase-locked loop. Alternatively, a delay circuit may be used to delay only one or both of first and second charge pump control signals from being supplied to the reset logic. If both the first and second charge pump control signals are delayed, a different delay time is used for each.

As described in the specification on page 12, lines 5-13, the asymmetric delay in the reset path corresponds to fractional-N divider jitter. In practice, this jitter is, for example, approximately 3 RF cycles, or 1.6 - 3.3ns for RF frequencies in the range 900-1800MHz (such as in a GSM system). According to claim 1, the phase detector output is linear with respect to the phase difference between the first and second signals (as illustrated by Fig. 11, for example). As illustrated by Fig. 10, an up-down current balance in the phase detector prevents noise folding. In practice, however, a

small imbalance will exist (see Fig. 6) and delta-sigma induced phase jitter (see Fig. 9) will cause noise folding even when the up-down current pulses are timed accurately. That is, when the reference leads the feedback signal by a certain amount, the error current is not identical in magnitude as in the case when the feedback leads the reference by the same amount.

To circumvent this even-order nonlinearity in the phase detector, the phase detector of claim 1 shifts the operating point of the phase detector so that a nonzero output signal corresponds to a nonzero phase difference between the first and second signals. This moves the operating region for the delta-sigma jitter, *during phase-locked conditions*, to one charge pump side.

For example, as illustrated in Fig. 11, the operating point is shifted to point 1101 and away from the nonlinearity at the origin 1103. Therefore, operation is moved substantially away from the origin 1103, where there are nonzero output signals and corresponding nonzero phase differences.

For the foregoing reasons, the claims are believed to be sufficiently enabling. As no outstanding art rejections have been asserted, Applicant believes the application to be in condition for allowance, and a Notice of Allowance is earnestly solicited. If any questions remain, please call the undersigned at the below-listed telephone number.

Respectfully submitted,

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I hereby certify that this correspondence is being sent by facsimile transmission to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 to the following facsimile number:

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